System Level Laboratory

Digital Fundamentals: Implement comparator using pSoC

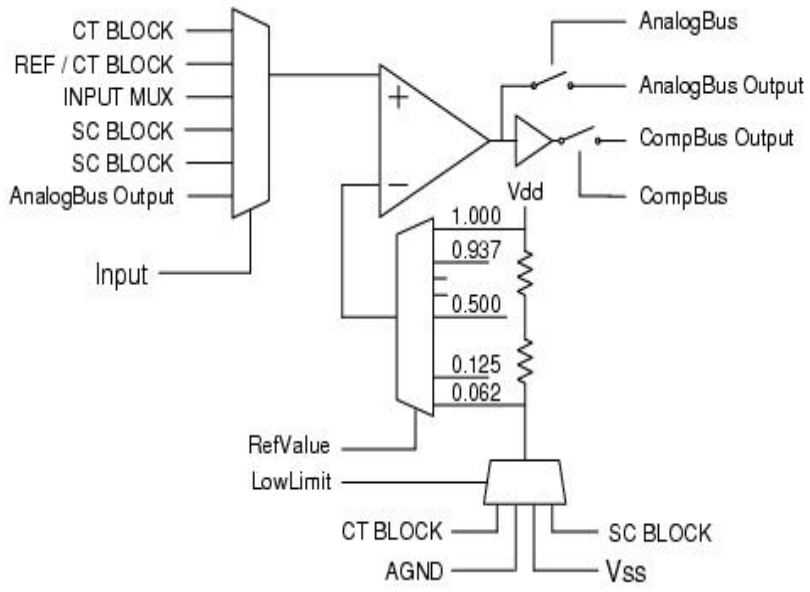
Objective:

Now that you are familiar with the Programmable System-on-chips (PSoC) and its development environment, we will learn in this experiment more detail about the comparator function block CMPPRG and use it to build a comparator by configuring the function block.

1. Digital Comparator Block: CMPPRG

Features and Overview:

The CMPPRG User Module provides a comparison of the selected input voltage against a programmable reference threshold (V_{TH}). Its programmable threshold is determined by the reference value (Vref), the power supply (Vdd), and the Low Limit value user provides. It has direct connection to other digital PSoC blocks as well as the interrupt block. The speed of the comparator can be adjusted by programming the power level of the Op Amp in the PSoC block – see CMPPRG block diagram below:



CMPPRG Functions:

The comparator is constructed from a continuous time OpAmp with the internal compensation capacitor disabled. Its positive input is connected to the input multiplexer. Its negative input is connected to the tap of a resistive divider between Vdd and the selected reference, Low Limit. When Low Limit is connected to AGND, there is an error term due to offset voltage. When Low Limit is connected to Vss, this error term is zero and thresholds will be slightly more accurate. The input range and the RefValue (effective threshold) are limited by the value of threshold. The threshold value of the comparator is determined by the following equation:

$$V_{TH} = LowLimit + (V_{dd} - LowLimit) \cdot V_{ref}$$

The output of the comparator can be accessed in two ways: the direct analog output or the comparator logic output. The logic output can be switched onto the Comp Bus to drive and enable inputs of digital blocks, the interrupt controller, and a register that can be read by the CPU.

Note: The frequency of the column clock should be selected to be at least two to four times faster than the bandwidth of the incoming comparator signal. If the analog column clock is set to low, the comparator may not catch fast input transients.

Parameters and References:

- Input: Six sources can be selected as inputs. They are pin input multiplexer, analog CT block outputs, SC block outputs, Internal reference and the analog output bus.
- Low Limit (V_{Low}): The reference low limit can be selected from fixed threshold sources like Analog Ground(AGND) and Vss or variable threshold sources like continuous time PSoC block or switched capacitor PSoC block.
- RefValue (Vref): When the V_{Low} is selected at Vss and operating from a 5V supply, the Vref is set to a value from 0.3125V to 5.0V with step change of 0.3125V. If the V_{Low} is set as AGND, the Vref will vary from AGND(2.6V) + 0.150V to 5.0V in steps of 0.15V.
- Comp Bus: The output from Comp Block comparator can be connected to adjacent PSoC digital blocks or to an interrupt. Note: The Comp Bus must be enabled to make the connection.
- Analog Bus: The Comp block comparator output can be connected to Analog Bus so that we can have a direct logic output signal. This signal is routed to output pin through Analog Buffer.

Application Programming Interface:

1. CMPPRG_Start**:** Perform all required initialization for this module and set the power level for the continuous time PSoC block. The comparator output will be driven
2. CMPPRG_SetPower: Set the power level for the continuous time PSoC block. The comparator output will be driven. May be used to turn the block off and on.
3. CMPPRG_SetRef: Set the reference value for the comparator.

4. CMPPRG_Stop: Turn the user module off. The output will not be driven

A basic comparator block in action is shown below: